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US 4441074 A

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UK CL (Edition L) G4A AEC AEX
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(54) **Bit error-rate testing.**

(57) A bit error-rate tester (10) has an XOR comparator (14) for comparing an input bit stream (12) with a reference bit stream (16) and for locating error bits in the input stream which differ from corresponding bits in the reference stream, and a display (26, 32) for displaying a result of the comparison. The display (32) has: a first section displaying a sequence of bits of the input stream occurring prior to an error bit; a second section displaying the error bit; and a third section displaying a sequence of bits of the input stream occurring after the error bit.

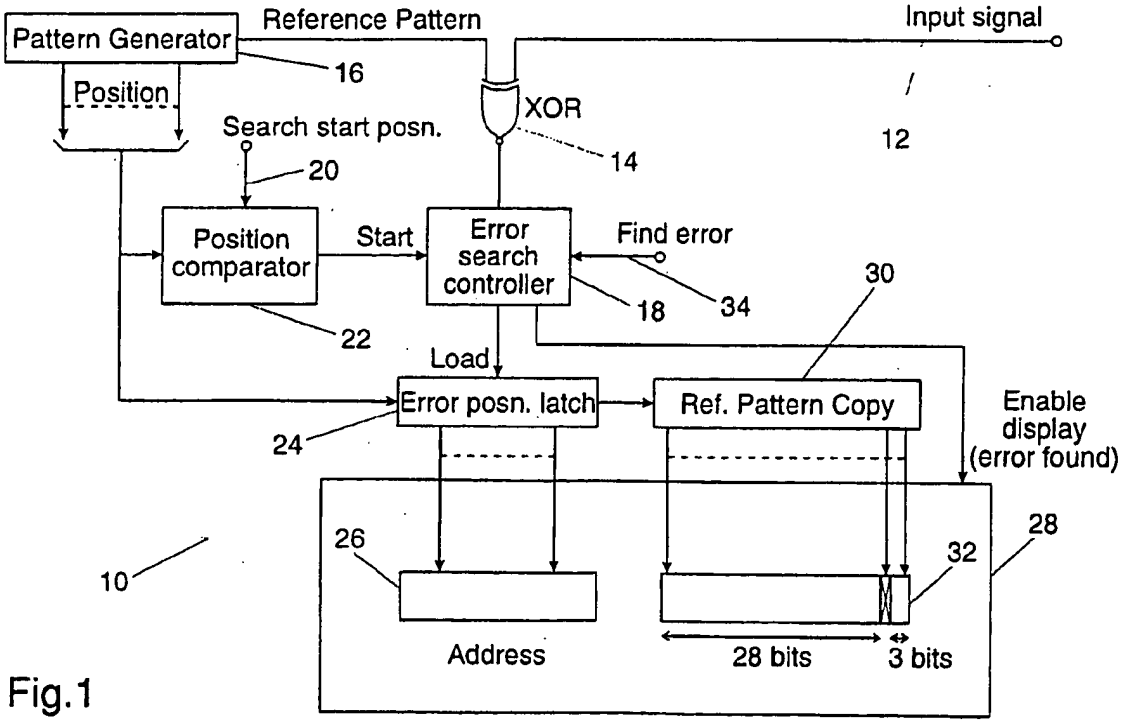

Fig.1

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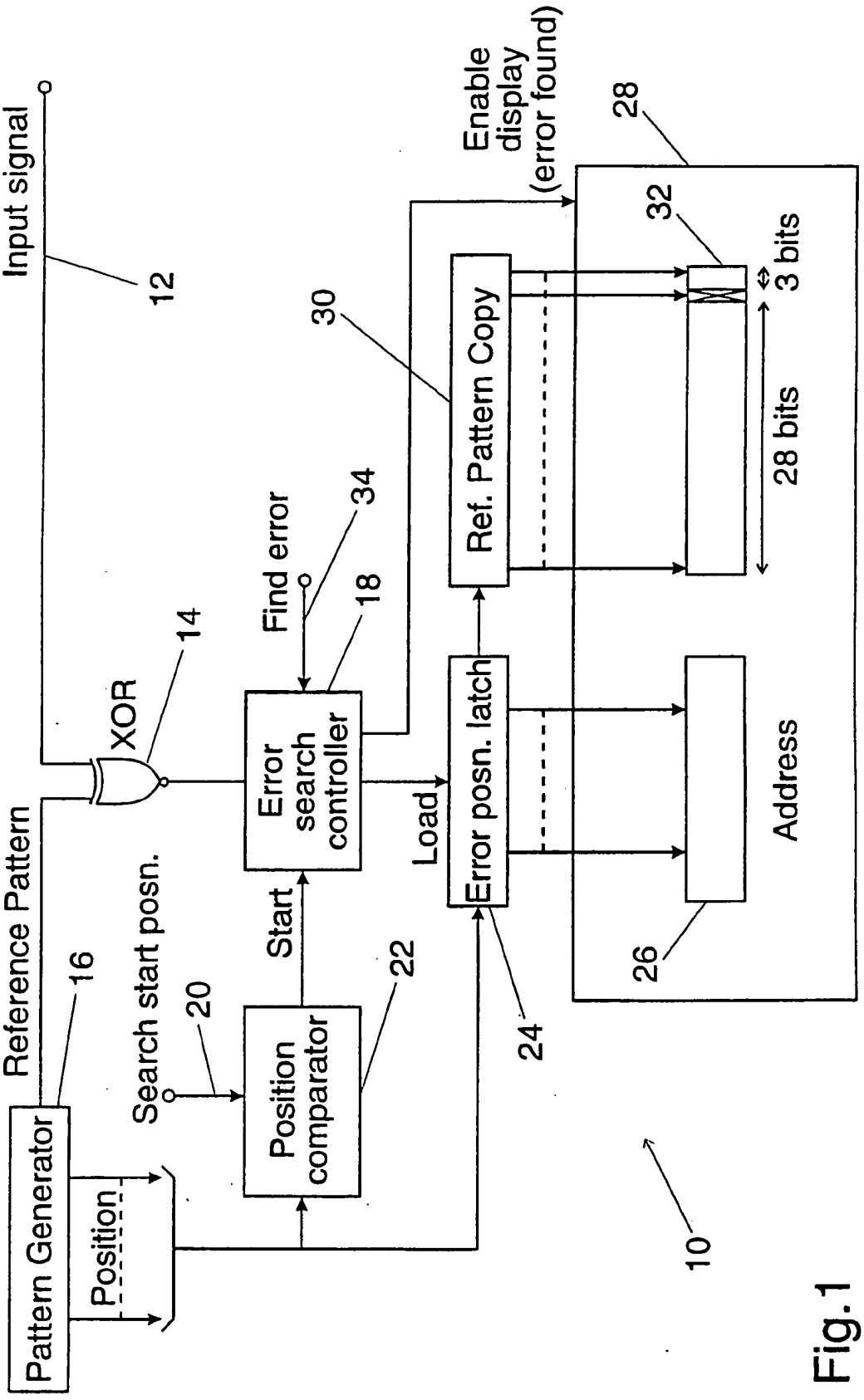
Input signal
12
Enable display (error found)
28
32
3 bits
28 bits
30
Ref. Pattern Copy
Find error
34
18
14
XOR
Error search controller
Load
Error posn. latch
Address
Reference Pattern
16
Search start posn.
20
Start
22
Position comparator
24
26
Pattern Generator
Position
10

Fig.1

Bit error-rate testing

Technical Field

This invention relates to bit error-rate testers (BERTs).

Background Art

An important parameter for assessing the quality of a binary digital communications link is its bit error rate (BER), that is the probability that a bit is incorrectly detected by a receiver. The BER is typically measured by transmitting over the link a long quasi-random test sequence of bits, and counting how many are incorrectly received. Correct or incorrect reception may be determined by generating a known correct sequence in a tester located adjacent the receiver, and comparing this sequence with the sequence received over the communications link.

Known BERTs merely provide an indication of the proportion of bits which are incorrectly received. It is an object of this invention to provide a BERT which indicates additional information which may facilitate identification and correction of causes of errors in received binary digital signals.

Disclosure of Invention

According to one aspect of this invention there is provided a bit error-rate tester comprising means for effecting a comparison of an input bit stream with a reference bit stream and for locating error bits in said input stream which differ from corresponding bits in said reference stream, and display means for displaying a result of said comparison, said display means comprising:

a first section displaying a first predetermined number of bits of said input stream occurring prior to an error bit;

a second section displaying said error bit; and

a third section displaying a second predetermined number of bits of said input stream occurring after said error bit.

Brief Description of Drawings

A bit error-rate tester in accordance with this invention will now be described, by way of example, with reference to the accompanying drawing, in which:

Figure 1 is a block schematic diagram of the tester.

Best Mode for Carrying Out the Invention, & Industrial Applicability

Referring to Figure 1, a bit error-rate tester 10 includes an input terminal 12 for receiving an input stream of binary digital signals whose bit error rate is to be measured.

This input terminal is coupled to one input of an exclusive-OR gate 14, which is used as a comparator to detect differences between the input signal stream and a reference digital signal stream or pattern supplied to the other input of the gate 14 from a reference pattern generator 16. The pattern generator 16 may be, for example, a random-access memory (RAM) storing a sequence of bit patterns which are selected for output in accordance with address signals supplied to the memory; alternatively the generator may be a pseudo-random binary sequence (PRBS) generator of known design based on a shift register with feedback connections from its output to selected ones of its stages.

The output of the exclusive-OR gate 14 is coupled to an error search controller 18, the design and operation of which will be evident from the following description, and which also receives a 'Start' signal from a position comparator 20. This comparator in turn receives a position signal from the pattern generator 16 and an externally-supplied 'Search-start position' signal, on an input 22, defining a position from which searching for error bits is to start. If the pattern generator 16 is RAM-based, these position signals comprise the addresses of storage locations in the RAM; in the case of a PRBS generator, these signals comprise the contents of the PRBS shift register.

The position signal from the pattern generator 16 is also supplied to an error position latch 24 which has a 'Load' input controlled by the controller 18. The contents of this latch are in turn supplied to an address portion 26 of a display 28 and to a pattern copy generator 30 which can output a total of thirty-two bits in parallel to a data portion 32 of the display 28.

If the pattern generator 16 is RAM-based, the copy generator 30 is likewise RAM-based and stores the same bits patterns as the generator 16. The copy generator 30 is arranged to output the (error) bit corresponding to the address in the latch 24, and also the twenty-eight bits corresponding the immediately-preceding twenty-eight addresses and the three bits corresponding to the immediately-following three addresses. If the pattern generator 16 is a PRBS generator, the copy generator 30 incorporates a similar shift-register based circuit. The copy generator 30 is in this case arranged to step backwards through twenty-eight shift register states, to generate the twenty-eight bits immediately preceding the error bit, and forwards through three shift register states, to generate the three immediately following bits. In either case, the copy generator 30 may be arranged to receive data from the pattern generator 16 to enable it to reproduce as and when required the digital signal pattern provided by the pattern generator 16.

The display 28 is controlled to provide visible indications in its address and data portions 26 and 32 in response to an enable signal from the controller 18. The controller itself has an input 34 for receiving an externally-supplied 'Find error' signal.

When a test is to be performed, the position within the reference signal pattern at which error detection is required to start is specified via the input 20. The pattern

generator 16 is synchronized with the input signal in known manner, and the 'Find error' signal on the input 34 is enabled.

The pattern generator 16 supplies the reference pattern to the exclusive-OR gate 14, which compares it with the input signal received on the input terminal 12. Any differences between the two signals will cause the exclusive-OR gate to supply an error signal to the error search controller 18; however, until the 'Start' signal is received from the position comparator 22, the controller 18 ignores this error signal.

When the position signal from the pattern generator 16 reaches the position specified via the input 20, the 'Start' signal is supplied to the controller 18. Thereafter the occurrence of any error signal will cause the controller 18 to enable the 'Load' input of the latch 24 and the enable-display input of the display 28. As a result, the pattern position at the time of occurrence of the error signal is stored in the latch 24, and displayed as an address in the address portion 26 of the display 28.

In addition, the contents of the latch 24 are used by the pattern copy generator 30 as described above to provide a display in the address portion 32 of the display 28 of the bit value which caused the error (the error bit), together with the twenty-eight bits preceding it and the three bits following it. We have found that providing this information about the sequence of data bits occurring before and after the error bit, in addition to the address of that bit, significantly assists interpretation of the error information and identification of the cause.

The tester may be further arranged to repeat the test multiple times, and measure the bit error rate for the error bit position, for example by repeating the above-described generation of the test pattern (in the vicinity of the position of the error bit) and comparison with the input signal multiple times, and determining the ratio of total occurrences of errors which occur specifically at the error bit position to the total number of tests. This may be done, for example, by using conventional bit error rate measurement circuitry, but controlled to count errors only if they occur at the error bit position. If the measured error ratio is relatively low, the error is likely to be random in nature; however, if the measured error ratio is relatively high, then a systematic error condition is indicated which warrants further investigation.

CLAIMS

1. A bit error-rate tester comprising means for effecting a comparison of an input bit stream with a reference bit stream and for locating error bits in said input stream which differ from corresponding bits in said reference stream, and display means for displaying a result of said comparison, said display means comprising:
a first section displaying a first predetermined number of bits of said input stream occurring prior to an error bit;
a second section displaying said error bit; and
a third section displaying a second predetermined number of bits of said input stream occurring after said error bit.

2. The bit error-rate tester of claim 1, wherein said display means includes a fourth section displaying the location in said input stream of said error bit.

3. The bit error-rate tester of claim 1 or claim 2, wherein said comparison is repeated a plurality of times and a bit error rate is determined for errors occurring at the location in said input stream of said error bit.

4. The bit error-rate tester of any one of the preceding claims, wherein said first predetermined number is twenty-eight, and said second predetermined number is three.

5. A bit error-rate tester substantially as hereinbefore described with reference to the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report) -5-

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Relevant Technical fields

(i) UK Cl (Edition L) G4A (AEC, AEX); H4P (PEX)

(ii) Int Cl (Edition 5) G06F 11/26

Search Examiner

S J PROBERT

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

14 SEPTEMBER 1993

Documents considered relevant following a search in respect of claims 1-5

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	US 4441074 (BOCKET-PUGH ET AL) see whole document	1

SF2(p)

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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